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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,484	03/12/2004	Chan-kyung Kim	SEC.1122	6300

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,484	KIM, CHAN-KYUNG	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *5-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (U.S. Patent No. 6,342,801).

In reference to claim 1 Shin discloses in Figure 5 a duty cycle correction circuit of a delay locked loop comprising: a differential amplifier (432), having first and second input terminals and first and second differential output terminals, and adapted to receive differential reference clock signals (clki, clkib) input via the first and second input terminals, to amplify the differential reference clock signals (clki, clkib), and to output the amplified differential reference clock signals via the first and second differential output terminals; a first transmission circuit (P9, N19), connected between the first differential output terminal of the differential amplifier (432) and a first node (N16), and adapted to transmit to the first node a first one of the amplified differential reference clock signals appearing at the first differential output terminal of the differential amplifier; a second transmission circuit (N20, P12), connected between the second differential output terminal of the differential amplifier and a second node (N17), and adapted to transmit to the second node (N17) a second one of the amplified differential reference clock

signals appearing at the second differential output terminal of the differential amplifier; a first storage unit (N23) connected between the first node (N16) and a ground voltage and adapted to store a signal of the first node; a second storage unit (N27) connected between the second node (N17) and the ground voltage and adapted to store a signal of the second node; and a switching circuit (P13, N24, P14, INV9, P15, N28, P16, INV10) connected between the first node (N16) and a first output terminal of the duty cycle correction circuit, and connected between the second node (N17) and a second output terminal of the duty cycle correction circuit, the switching circuit having a control terminal adapted to receive a switching control signal (pdn) to selectively provide the signals of the first and second nodes to the first and second output terminals of the duty cycle correction circuit. The same applies to claims 13-16n wherein the integrating means is equivalent to the first and second storage units (N23, N27) and the switching means (P13, N24, P14, INV9, P15, N28, P16, INV10) selectively outputs the control signals (the signals of the first and second nodes, with reference to claim 1) when the switching control signal (pdn) has a first state and to output a pair of fixed voltage signal (vssA) when the switching control signal has a second state, the fixed voltage signals are ground voltages and the switching means includes a pair of transistors (N25, N29) connected between corresponding output terminal and ground.

In reference to claim 2 Shin discloses in Figure 5 wherein the switching circuit comprises a third transmission circuit (N24, P14) adapted to transmit the signal of the first node (N16) to the first output terminal when the switching control signal (pdn) has a deactivated state; a fourth transmission circuit (N28, P16) adapted to transmit the signal

of the second node (N17) to the second output terminal when the switching control signal (pdn) has the deactivated state; a first voltage supplying circuit (N25) which is connected between the first output terminal and the ground voltage, and supplies the ground voltage to the first output terminal when a switching control signal (pdn) has an activated state; and a second voltage supplying circuit (N29) which is connected between the second output terminal and the ground voltage, and supplies the ground voltage to the second output terminal when the switching control signal has the activated state.

In reference to claim 3 Shin discloses in Figure 5 wherein the first through fourth transmission circuits (P9, N19; N20, P12; N24, P14; N28, P16) each include a PMOS transistor and a NMOS transistor.

In reference to claim 4 Shin discloses in Figure 5 wherein each of the first storage unit (N23) and the second storage unit (N27) is a MOS transistor.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

CC

November 26, 2005

/Kenneth Wells/

Kenneth B. Wells
Primary Examiner